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A Novel Hybrid Converter with Simultaneous DC and Three Phase AC Outputs

Anil J Thomas[1], Ajitha Tomy[2]

Assistant Professor, Dept. of EEE, Federal Institute of Science and Technology, Angamali, Kerala, India[1]

PG Student [PEPS], Dept. of EEE, Federal Institute of Science and Technology, Angamali, Kerala, India[2]

ABSTRACT:A novel hybrid converter topology called Sepic Derived Hybrid Converter (SDHC) which is capable of providing step up/step down DC output and three phase AC output simultaneously is proposed. This topology is called 3-φ Sepic Derived Hybrid Converter (3-φ SDHC).The main advantage of this architecture is inherent shoot through protection compared to conventional Voltage Source Inverters (VSI)which avoid dead time compensation. The other advantages include high power processing density, well co-ordination of power flow to both outputs, independent regulation of AC and DC outputs etc. The validity and effectiveness of proposed hybrid converter are verified by simulation using MATLAB SIMULINK.

KEYWORDS: Shoot through, Hybrid Converter, Power processing density.

I.INTRODUCTION

Now a days there is a growing need for highly reliable supply of electrical energy for critical applications such as hospitals, datacom centres and semiconductor industry which has spawned the development of super-reliable local power distribution system with extended use of power electronic converters. These systems include multiple primary and secondary energy sources, several levels of energy storage and back-up, and numerous active loads, all interfacedthrough power electronic converters. Similarly, there has been increased incorporation of power electronic converters in electric cars, ships, and airplanes. The goals have been to reduce the size, weight, maintenance and operational costs of these power systems, while increasing efficiency, safety, reliability, and optimizing mission-specific objectives (payload, autonomy, survivability), as well as to enable the usage of alternative energy sources, e.g. fuel cells. In these applications, majority of energy sources are interfaced to the system through power electronic converters because of their very different dynamic characteristics. When both DC and AC loads are present, conventionally many DC-DC power converters or a multi-output DC-DC converter is used and voltage source inverter (VSI) stages are cascaded to DC-DC converters to provide AC output.

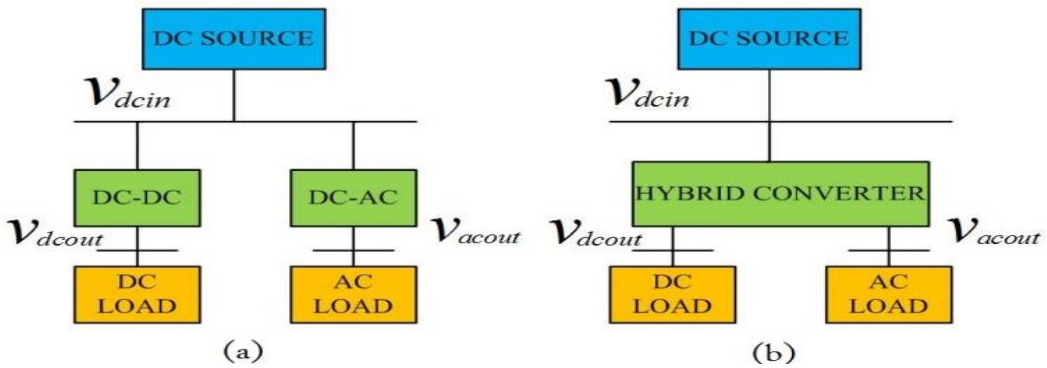

Fig. 1: Architecture with single dc input and simultaneous
DC and AC outputs. (a)Power converter based architecture. (b)Hybrid converter based architecture.

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Fig 1 shows the schematic of multioutput system which comprises both DC and AC load. The Fig 1(a)represents separatestages for DC-DC and DC-AC conversion whereas Fig 1(b)usessingle stage to perform both conversions. The latter is called hybrid converter which has higher power processing density, improved reliability, and inherent shoot through protection. Thesequalities make them suitable for compact power system with both DC and AC loads.

II.PROPOSED ARCHITECTURE

This architecture of hybrid converter [shown in Fig 2] is derived from Single Ended Primary Inductor converter (SEPIC) by replacing the control switch by three phase bridge network. In conventional VSI turning ON of switches in same leg (Shoot through) result in short circuit. In order to avoid this there should be dead time compensation in switching signals which increases the harmonics. But in case of 3-φ SDHC shoot through is a switching interval and its duration decides the step up or step down operation of DC output. The shoot through state in the inverter improves the electromagnetic interference (EMI) tolerance of inverter and makes it more reliable.

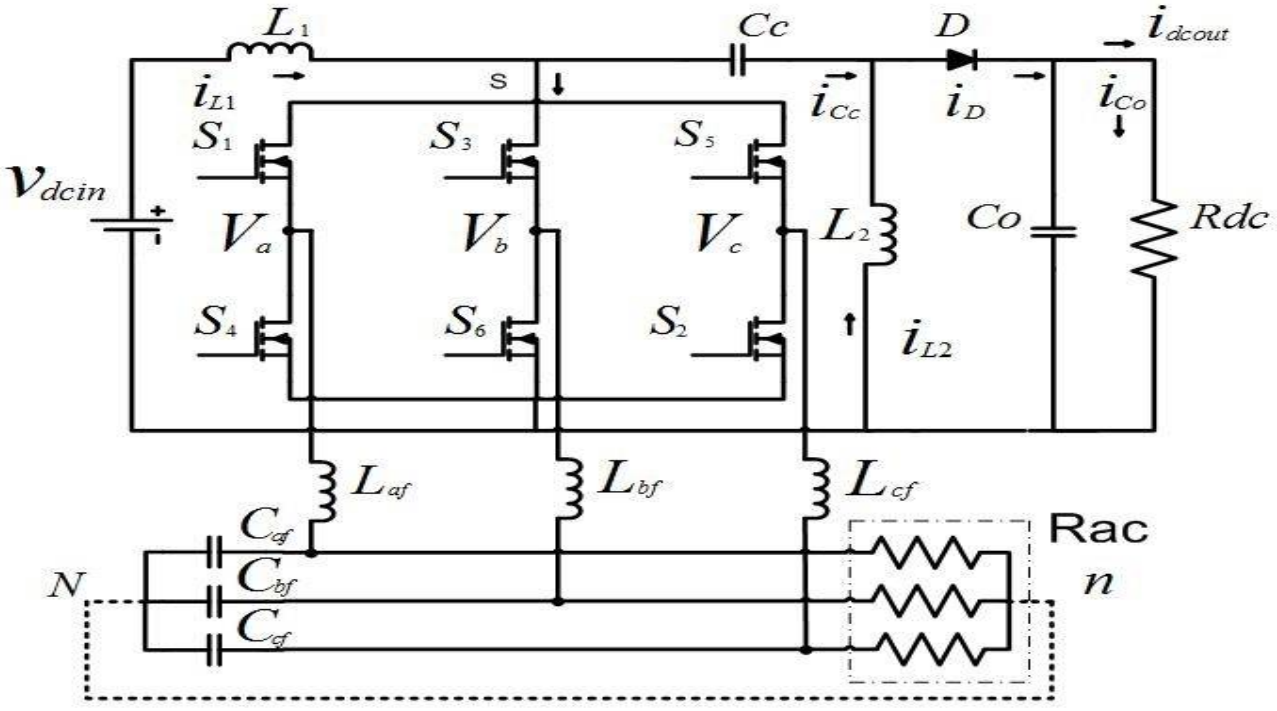

Fig 2: Circuit diagram of 3-φ SDHC. The switch realization for the bridge can be done using bidirectional switches- either IGBTs with antiparallel diode or MOSFET.

III.OPERATING PRINCIPLE OF 3-φ SDHC

There are six switches to control both DC and AC outputs as shown in Fig 2. The 3-φ SDHC mainly operate in three switching intervals: 1) Shoot through interval 2) Power interval 3) Zero interval. Equivalent circuit diagram for each of the switching intervals are given below. For steady state analysis continuous conduction mode is assumed.

- **Interval 1, Shoot through interval [Fig 3 and Fig 6]:** In this interval switches of one particular leg are turned ON. The duration of this interval decides the duty ratio (D_{st}) which in turn regulates the DC output. If D_{st} is less than 0.5 there will be a step down DC output and if D_{st} is greater than 0.5 there will be step up DC output. This interval is analogous to turning ON the control switch of SEPIC converter. Here the inductor L_1charges from DC supply and inductor L_2 charges from previously charged coupling capacitor C_c . The diode D is reverse biased and DC output is supplied by output capacitorC_{out}.

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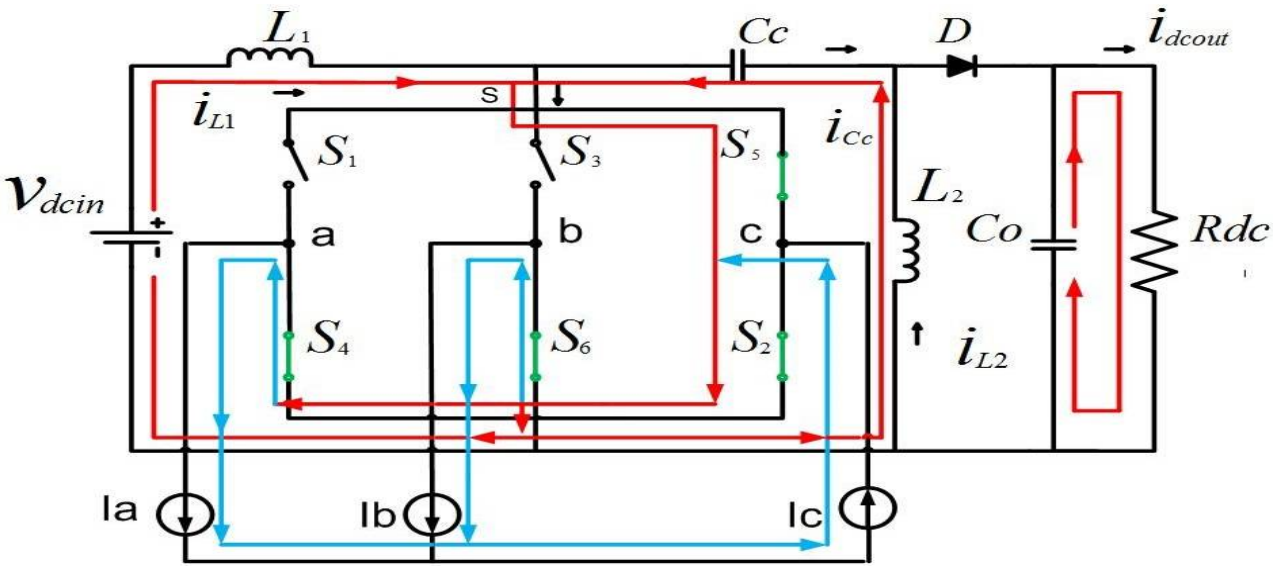

Fig 3: Equivalent circuit diagram of 3-φ SDHC in Shoot through interval.

- **Interval 2, Power interval [Fig 4 and Fig 6]**: In this interval two top or bottom switches and opposite switch of remaining leg is turned ON. The inverter bridge network gets connected to a voltage of $V_{dcin} + V_{dcout}$ in this interval where $V_{dcin}$is the average voltage across the coupling capacitorC_c.The DC source and input inductor supplies AC load current as well as charges coupling capacitor. The diode D is forward biased in this interval.

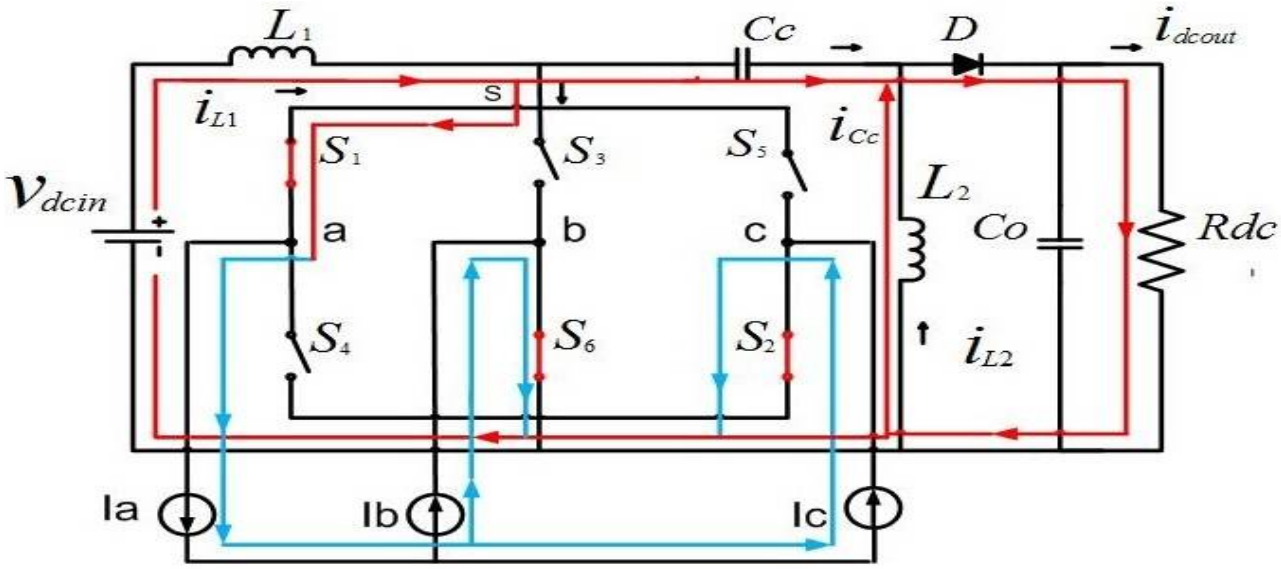

Fig 4: Equivalent circuit diagram of 3-φ SDHC in Power interval.

- **Interval 3, Zero interval [Fig 5 and Fig6]**: In this interval, either all the top or bottom switches are turnedON. The inductors (L_1 *and* L_2) continue discharging and the diode D is forward biased.

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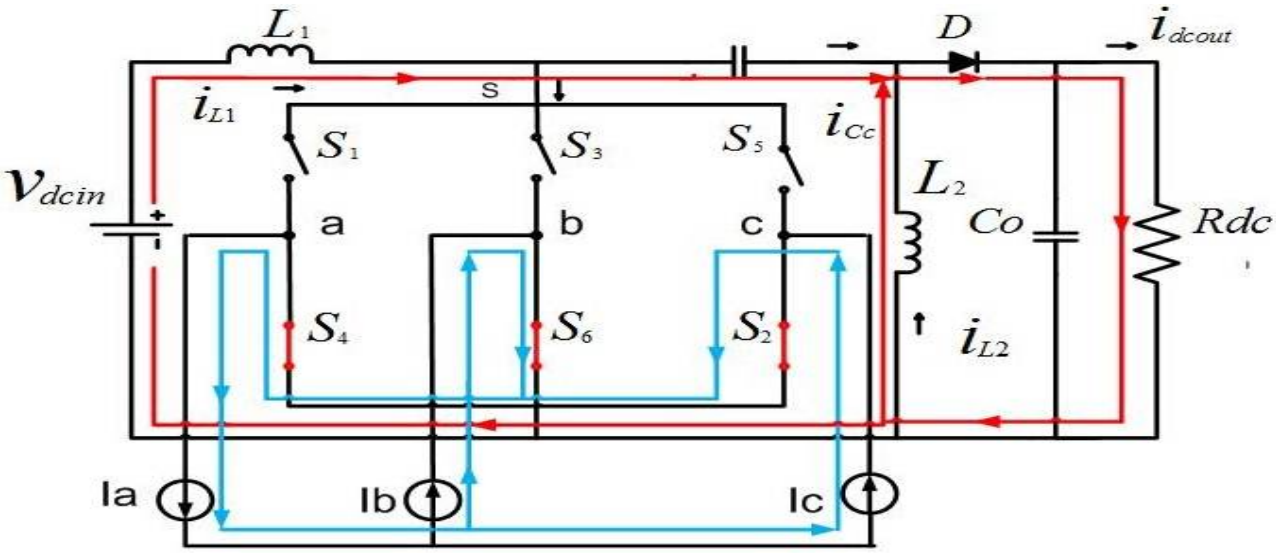

Fig 5: Equivalent circuit diagram of 3-φ SDHC in Zero interval.

IV.STEADY STATE ANALYSIS

The DC gain achieved by 3-φ SDHC is same as conventional SEPIC converter and is given by:

$$\frac{V_{dcout}}{V_{dcin}} = \frac{D_{st}}{1 - D_{st}} \quad ----------(1)$$

The RMS value of line to line AC output voltage can be expressed as:

$$\frac{V_{acout}}{V_{dcin}} = 0.612 * \frac{M_a}{1 - D_{st}} \quad ---------(2)$$

Where M_a is the modulation index. From equation (1) and (2) we can conclude that DC output depends only on duty ratio whereas AC output depends on both duty ratio and modulation index. The equations (4) and (5) give expressions for DC output power P_{dc} and AC output power P_{ac}.Here the DC load and AC load considered are purely resistive and equal to R_{dc} and R_{ac} respectively.

$$P_{dc} = \frac{V_{dcin}^2 * D_{st}^2}{R_{dc}(1 - D_{st})^2} ----------(3)$$

$$P_{ac} = \frac{V_{dcin}^2 * 3 * M_a^2}{4 * R_{ac}(1 - D_{st})^2} ----------(4)$$

In this topology the AC and DC power co-ordination are achieved by same set of switches. Hence there is a constraint in the switching strategy given by

$$M_a + D_{st} \leq 1 ----------(5)$$

At the condition of equality of relation (5), the RMS value of the output ac voltage is equal to 0.612times V_{dcin} independent of modulation index and duty ratio. This is equal to that achieved using a conventional 3-phase VSI topology.

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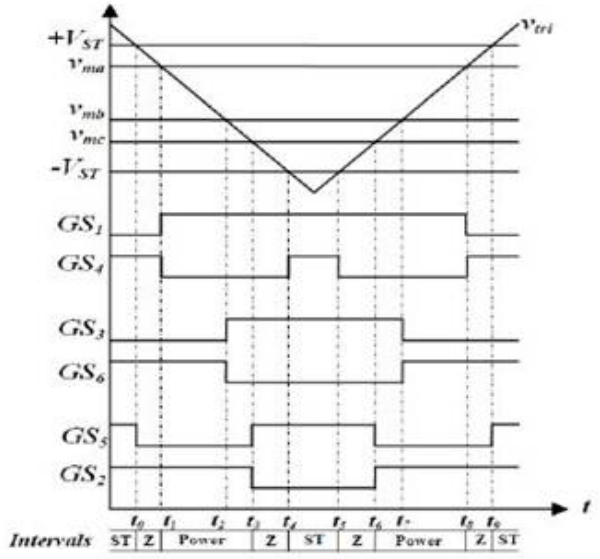
V. CONTROL SCHEME

The Constant Frequency Shoot through Sine Pulse Width Modulation (CFST-SPWM) control strategy is based upon the control scheme proposed in [2],is used in this architecture. In this scheme, depending upon the relative magnitudes of the phase voltages, the shoot-through interval is executed by any particular leg.The PWM control circuit requires five references: $v_{ma,}v_{mb,}v_{mc}$ which regulate the ac output, $+V_{ST}$, and $-V_{ST}$ regulates the dc output voltage. Fig. 7 shows the schematic for realization of the PWM control signals for the proposed converter shown in fig 6.



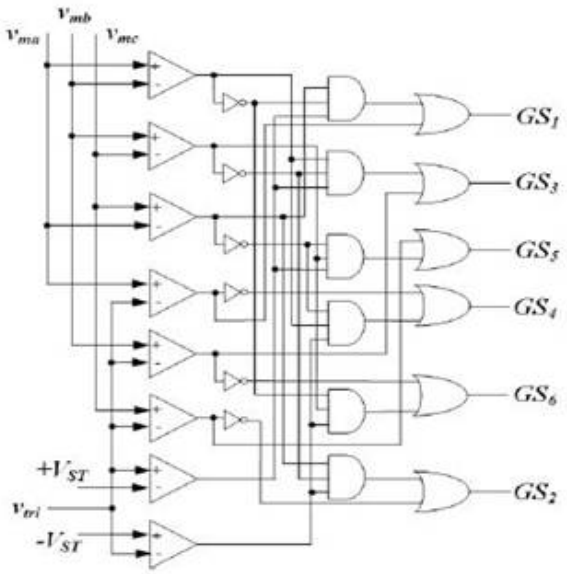


Fig 6 :CFST-SPWM based control scheme for 3-φ SDHC Fig 7: Implementation of CFST – SPWM.

V.SIMULATION RESULTS

The steady state behaviour of the novel topology is verified using MATLAB SIMULINK. The experimental specifications and design specifications are given in Table 1 and Table 2.The figures below shows the output wave forms for different duty ratio and modulation index.

Parameter	Attributes
Input Voltage	24V
DC output voltage	12 – 40 V
AC output voltage (RMS)	10V
Switching frequency	20KHz
AC and DC load	100Ωper phase

Table 1: Parameter specifications

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Component	Attributes
Inductors(L_1 and L_2)	4.7mH
Coupling capacitor(C_c)	470µF
Output capacitor (C_{out})	2.2mF
AC filter capacitor(C_{af}, C_{bf} and C_{cf})	10µF per phase
AC filter inductor(L_{af}, L_{bf} and L_{cf})	250µH per phase

Table 2: Component specification.

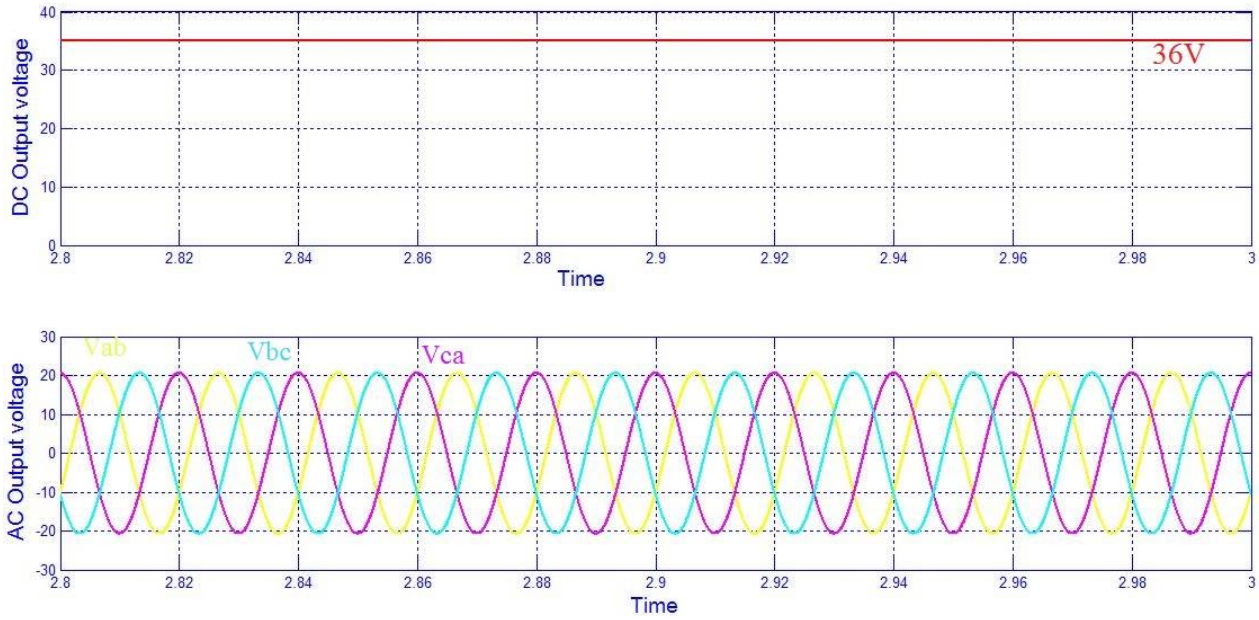

Fig 8: DC and AC output (line voltage) waveforms for D_{st}=0.6 and M_a=0.4

Fig 8 shows the simulation result of 3-φ SDHC for duty ratio D_{st} equal to 0.6 and Modulation index M_a equal to 0.4.Since the criteria mentioned in equation (5) is maintained at equality the rms value of AC output voltage is 0.612 times DC input voltage. The harmonics in AC output is less than 1% which is analysed using FFT tool of MATLAB.The value of D_{st} is greater than 0.5 therefore boost operation occurred in the DC output. The AC output waveform shown are line voltagesV_{ab},$V_{bc}$and V_{ca}.

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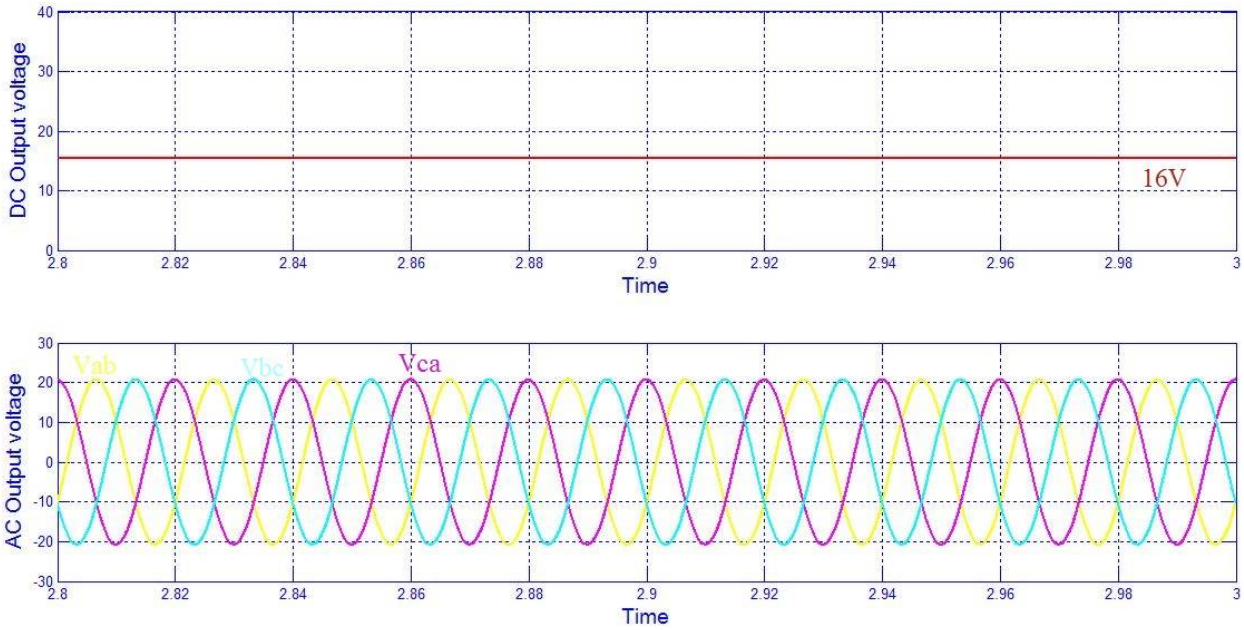

Fig 9: DC and AC output (line voltage) waveforms for D_{st}=0.4 and M_a=0.6. (Buck mode)

Fig 9 shows the simulation result of 3-φ SDHC for duty ratio D_{st} equal to 0.4 and Modulation index M_a equal to 0.6.Since the criteria mentioned in equation (5) is maintained at equality the rms value of AC output voltage is 0.612 times DC input voltage. The harmonics in AC output is less than 1% which is analysed using FFT tool of MATLAB.The value of D_{st} is less than 0.5 therefore buck operation occurred.

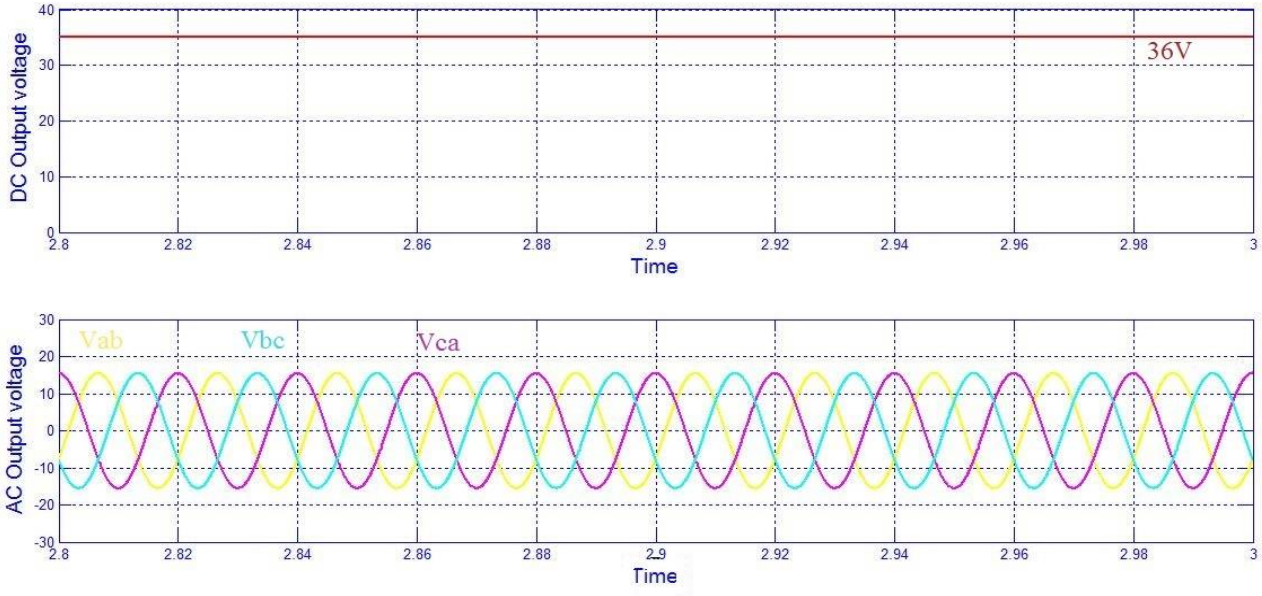

Fig 10: DC and AC output (line voltage) waveforms for D_{st}=0.6 and M_a=0.3(Boost mode).

Fig 10 shows the simulation result of 3-φ SDHC for duty ratio D_{st} equal to 0.6 and Modulation index M_a equal to 0.3. Here the criterion mentioned in equation (5) is maintained at less than 1. Therefore according to equation (2) peak

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value of AC output voltage should be 15.57 and it is verified in simulation. The FFT analysis of the line voltage V_{ab} in AC output waveform of Fig 10 is given in Fig 11.The harmonicsin AC output is less than 1%.

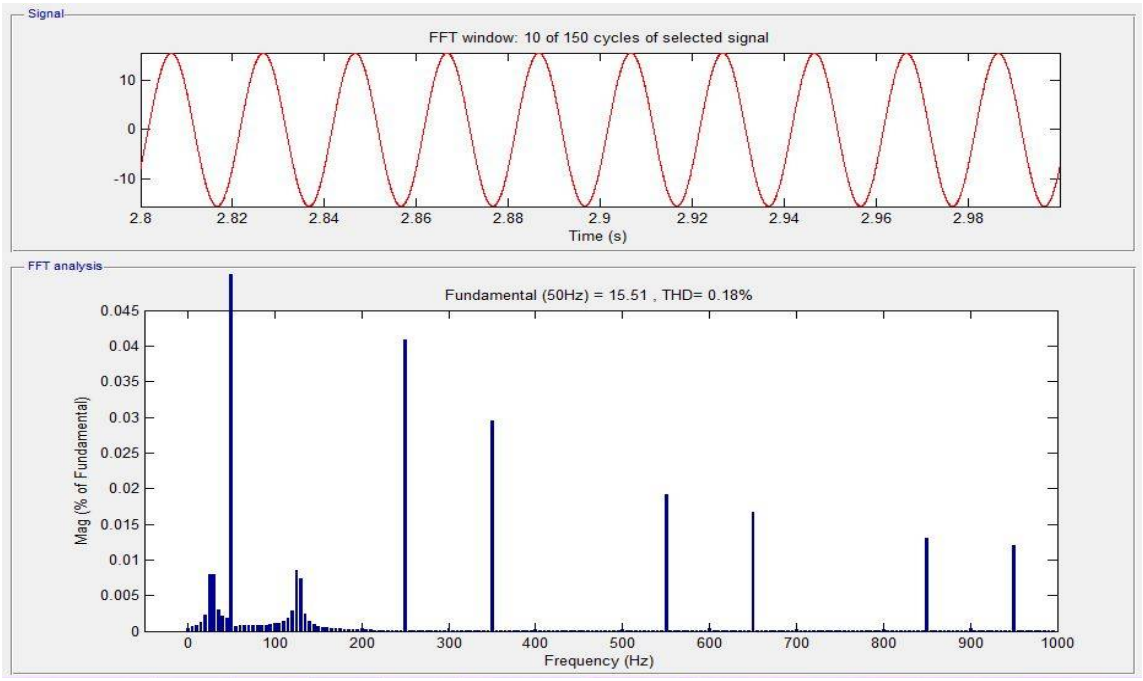

Fig 11: FFT analysis of the line voltage V_{ab} in the result shown in fig 10.

VI.CONCLUSION

A hybrid converter topology which provides three phase AC output and step up/step down DC output simultaneously with reduced number of switches is proposed. The new topology has inherent shoot through protection which make it reliable in EMI atmosphere. In addition it has high power processing density and effient co-ordination of power flow to DC and AC load. The behaviour of proposed topology is validated using MATLAB Simulink. The FFT analysis of AC output shows that the harmonic content is less than 1%.

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